Depletion-Merged FET Design in Bulk Silicon

ABSTRACT OF THE DISCLOSURE

Field effect transistors having reduced reverse body effects and reduced parasitic junction capacitance and a method of manufacture. The FET's comprise source/drain region pairs formed in said bulk silicon, each pair separated by a channel region. The depletion region associated with each of the source/drain regions of a pair are fully merged by selective ion implantation. A gate electrode is formed or deposited over the channel region of each FET in the normal manner.